REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1-12 are presently active in this application; Claim 1 having been amended and new Claims 11 and 12 added by the present amendment.

In the outstanding Office Action Claims 1-3, 5-7, 9-10 were rejected under 35 USC §103(a) as being unpatentable over Roohparvar (U.S. Patent 5,675,540) in view of Matsumoto et al (U.S. Patent 5,278,839); and Claims 4 and 8 were objected to as being dependent upon a rejected base claim, but otherwise allowable if rewritten in independent form.

Applicants acknowledge with appreciation the indication that Claims 4 and 8 include allowable subject matter if rewritten in independent form. In light of this indication, submitted herewith are new Claims 11 and 12 which correspond to original Claims 4 and 8 rewritten in independent form. Accordingly, no new matter has been added and in view of the indication of allowable subject matter, Claims 11-12 are believed to be in condition for allowance.

In light of the rejection on the merits, Claim 1 has been amended to clarify the claimed invention, and thereby more clearly patentably define over the cited art. To that end, amended Claim 1 clarifies that the claimed semiconductor device has a function verification capability including an internal verification block receiving and then storing a desired first input value and a desired cycle value being a timing to supply the first input value to a target verification block corresponding to the internal verification block, both values being for use in an operation verification according to execution of internal verification instructions being executed in synchronization with one stage in pipeline for the semiconductor device during the operation verification, and supplying the first input data to the target verification block

instead of a second input data being for use in a normal operation after a time indicated by the cycle time is elapsed after receiving and storing the first input data and the cycle value.

Thus, according to the present invention, an internal verification block receives and then stores a desired first input value and a desired cycle value and internal verification instructions are executed in synchronization with one stage in pipeline for the semiconductor device. As a result, the operator is capable of optionally choosing the first input value and the cycle value.

Turning now to the cited prior art, the outstanding Office Action states that "Roohparvar substantially teach the present invention and verification cycle, pre-programming cycle, and erase cycle." However, neither Roohparvar '540 nor Matsumoto et al. '839, teach or suggest an internal verification block receiving and then storing a desired first input value and a desired cycle value and internal verification instructions being executed in synchronization with one stage in pipeline for the semiconductor device.

Thus, according to the cited prior art references, the operator is not capable of optionally choosing the first input value and the cycle value, and the prior art fails to teach or suggest providing a programmer the capability to replace a certain specific signal with desired values to desired timing per 1 cycle to a base clock, as claimed. As a result, the applied prior art fails to teach the effect of the claimed invention, which makes easy verification of all blocks of the others to which the signal line relates, and analysis.

Consequently, in view of the present amendment and in light of the above comments, the pending claims are believed to be patentably distinguishing over the cited prior art and

are believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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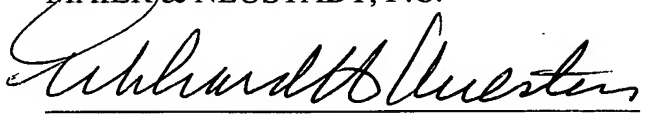

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